



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Keith A. Joyner, et al.

Docket No: TI-29912

Serial No: 10/068,014

Conf. No: 7239

Examiner: William M. Brewster

Art Unit: 2823

Filed: 02/05/2002

For: METHOD FOR MANUFACTURING AND STRUCTURE FOR TRANSISTORS WITH
REDUCED GATE TO CONTACT SPACING

2823
#6
Response
5/23/03
Mallish

AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(a)

I hereby certify that the above correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on 5-16-03.

Ann Trent
Ann Trent

Dear Sir:

Responsive to the Office Action mailed February 28, 2003, in connection with the above identified application, Applicants respectfully submit the following remarks.

RECEIVED
MAY 21 2003
TECHNOLOGY CENTER 2800